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MATERIALS SCIENCE

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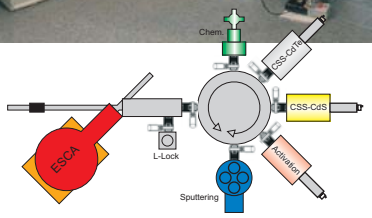
Integrated Systems for Solar Energy Research: First Results with DAISY-SOL

I. DAISY-SOL-Setup

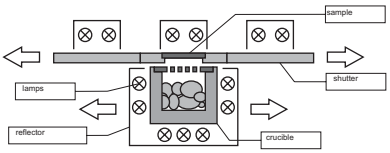
suported by the Federal Ministry for the Environment (contract number: 0329857A)

DAISY-SOL-CSS: Properties

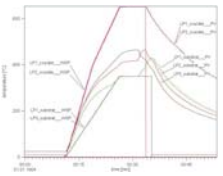
- \+ dynamic deposition (close to industrial manufacturing)
- \+ high rates of deposition (up to 10µm/min)
- \+ high substrate temperatures (up to 600°C)
- \+ homogeneous layers
- \+ only 2mm distance substrate/crucible
- – difficult temperature control
- – high CdTe-consumption (1g/layer)



- all in-situ solar cell manufacturing
- 2 dynamic CSS-chambers
- UHV-activation (in construction)
- backcontact formation (evaporation, sputtering)
- in-situ XPS/UPS-characterisation

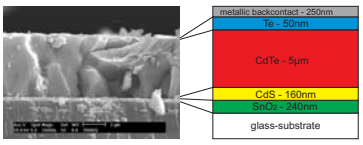


CSS-desposition-unit, schematic



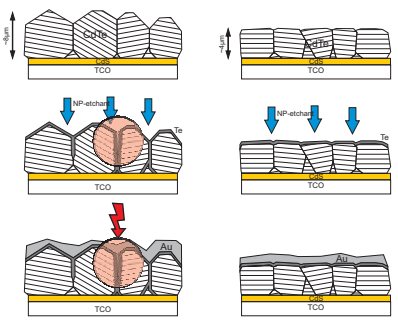
temperature-profile, CdTe-deposition

II. Investigations on Nucleation and Growth

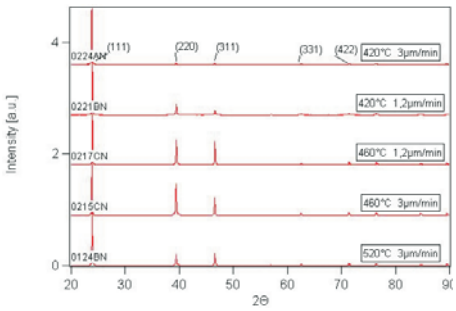


Requirements

At the present state CdTe-solar cells deposited with CSS-technique exhibit very large grains (>5µm) with high surface roughness (Rms>300nm). This usually leads to the formation of shunts during the activation process, etching and backcontact deposition.To avoid this, the CdTe-layer has to be thicker than 8µm, which is correlated with high efficiency losses due to a high series resistance. Our perspective is to reduce the surface roughness while maintaining a large grain size. Progress was made in modifying the morphology, grain size and roughness by variation of substrate temperature and growth rate. Furthermore investigations on texturing-dependent cell-performance were started.
As for the CdTe-layer similar behaviour depending on the surface roughnesses is observed for the CdS-layer. Holey CdS leads to direct contact of CdTe with the TCO, resulting in a low V_{OC}.

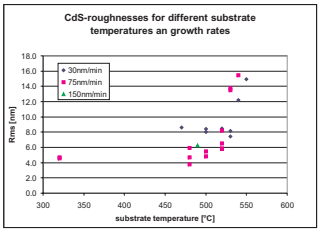


left: formation of shunts due to a high surface roughness and bad texturing
right: highly orientated, smooth CdTe-layer ensure uniform etching without shuntformation at grainboundaries. This allows reduction in CdTe-layerthicknesses.



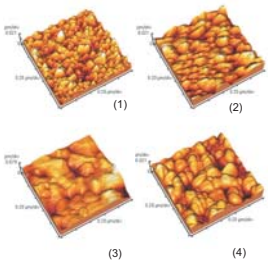
XRD-patterns for CdTe-layers deposited at different substrate temperatures and growth rates. For cooler substrates CdTe growth up strongly (111)-orientated. With increasing substrate temperature the preferred orientation switches to (220) and (311)-direction. It seems that higher deposition rates also influence the orientation to a more likely (111)-direction.

III. Morphology of CSS-CdS and CdTe Films

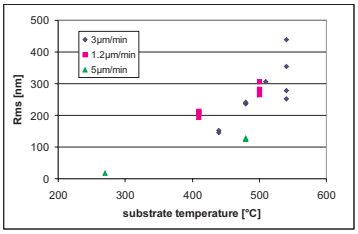


AFM-messurements on CdS-layers with similar thicknesses (d=150nm). CdS was deposited on SnO_2/In_2O_3-coated borosilicate glass.

- allmost constant roughness for substrate temperatures up to 520°C
- abrupt rise of roughness for temperatures above 520°C
- decreasing roughnesses for increasing growth rate

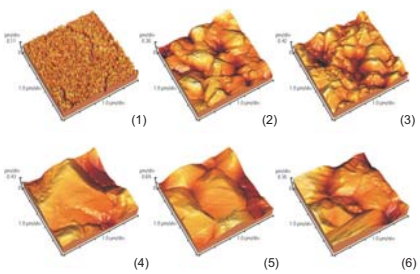


AFM-pictures of CdS-layers deposited with different substrate temperatures and growth rates. (1): T_{sub}=300°C, r_g=75nm/min; (2): T_{sub}=520°C, r_g=75nm/min; (3): T_{sub}=550°C, r_g=75nm/min; (4): T_{sub}=520°C, r_g=150nm/min



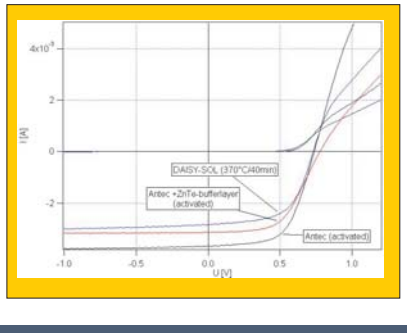
AFM-measurements on CdTe-layers with similar thickness (d~5µm). The roughness strongly depend on substrate temperatures and growth rates.

- increasing roughness for decreasing growth rates
- high spreading in roughnesses for high temperatures
- very smooth, almost mirroring, black colored layers for very low temperatures



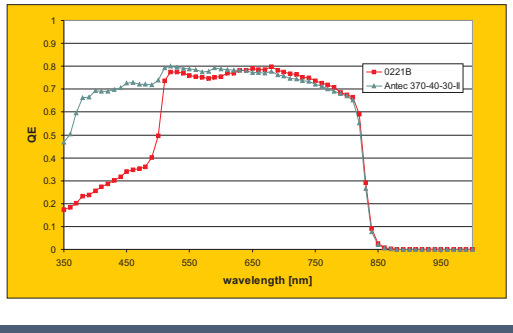
AFM-pictures of CdTe-layers deposited with different substrate temperatures and growth rates. (1): T_{sub}=270°C, r_g=5µm/min; (2): T_{sub}=480°C, r_g=5µm/min; (3): T_{sub}=440°C, r_g=3µm/min; (4): T_{sub}=510°C, r_g=3µm/min; (5): T_{sub}=410°C, rg=1,2µm/min; (6): T_{sub}=500°C r_g=1,2µm/min

IV. Electrical and Optical Characterisation



	DAISY-SOL cell	Antec-cell +ZnTe-layer	Antec-cell activated
(%)	8.34	8.48	11.07
V_{OC} (V)	0.73	0.776	0.736
J_{SC} (mA/cm²)	19.37	19.68	25.1
FF (%)	59	55.5	59.9

I/U-plots of activated CdTe-solar-cells
The plots labeled with ANTEC-cell refer to cells cut out from a modul out of ANTEC-production. One cell was covered with a ZnTe buffer layer before activation and backcontact-formation.
The activation process (in a tube furnace) was the same for all cells (T: 370°C, t: 40min). As backcontact we used sputtered gold.
The completely self deposited cell and the standard ANTEC-cell show similar voltages and fill-factors but slightly different currents what may be due to different CdS-layer thicknesses. The ANTEC-cell with the ZnTe-layer shows a much higher voltage but low voltage and a high series resistance which may be because of an unsufficient conductivity of the ZnTe/layer.



Quantum efficiency of DAISY-SOL solar cells vs. ANTEC-cells
The quantum efficiencies of both cells show good consistency for wavelenghts above the CdS-absorption edge (~510nm). The high values for the QE below 510nm for ANTEC-cells may explain the higher

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